CLAIMS

What is claimed is:

1. A method comprising:
detecting misaligned data access resulting from execution of a code block translated from a first format suitable for a first computing platform to a second format suitable for a second computing platform; and
modifying said code block according to said misaligned data access.

2. The method of claim 1, wherein detecting comprises performing instrumentation of said code block to detect whether execution of said code block results in the misaligned data access.

3. The method of claim 2, wherein detecting comprises performing instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access.

4. The method of claim 1, wherein detecting comprises performing instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access.

5. The method of claim 1, wherein modifying comprises adding to said code block an instruction to branch an execution of said code block to a code sequence whose execution handles the misaligned data access.

6. The method of claim 1, wherein modifying comprises modifying said code block to handle misaligned data access in a subsequent execution of said code block.

7. The method of claim 1, further comprising translating said code block from said first format to said second format.

8. The method of claim 1, wherein detecting comprises detecting a misaligned data access resulting from an execution of a code block translated from a format suitable for a 32-bit based computing platform to a format suitable for a 64-bit based computing platform.

9. An apparatus comprising:
a processor to detect misaligned data access resulting from execution of a code block translated from a first format suitable for a first computing platform to a second format suitable for a second computing platform, and to modify said code block according to said misaligned data access.

10. The apparatus of claim 9, wherein the processor is able to perform instrumentation of said code block to detect whether execution of said code block results in the misaligned data access.

11. The apparatus of claim 10, wherein the processor is able to perform instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access.

12. The apparatus of claim 9, wherein the processor is able to perform instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access.

13. The apparatus of claim 9, wherein the processor is able to add to said code block an instruction to branch an execution of said code block to a code sequence whose execution handles the misaligned data access.

14. The apparatus of claim 9, wherein the processor is able to modify said code block to handle misaligned data access in a subsequent execution of said code block.

15. The apparatus of claim 9, wherein the processor is able to, before detecting the misaligned data access, translate said code block from said first format to said second format

16. The apparatus of claim 9, wherein the first computing platform is a 32-bit based computing platform and the second computer architecture is a 64-bit based computing platform.

17. A computing platform comprising:
a processor to detect misaligned data access resulting from execution of a code block translated from a first format suitable for a first computing platform to a second format suitable for a second computing platform, and to modify said code block according to said misaligned data access; and
a dynamic random access memory operably associated with said processor to store at least a portion of said code block.

18. The apparatus of claim 17, wherein the processor is able to perform instrumentation of said code block to detect whether execution of said code block results in the misaligned data access.

19. The apparatus of claim 18, wherein the processor is able to perform instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access.

20. The apparatus of claim 17, wherein the processor is able to perform instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access.

21. A machine-readable medium having stored thereon a set of instructions that, if executed by a machine, cause the machine to perform a method comprising:
detecting misaligned data access resulting from execution of a code block translated from a first format suitable for a first computing platform to a second format suitable for a second computing platform; and
modifying said code block according to said misaligned data access.

22. The machine-readable medium of claim 21, wherein the instructions that result in detecting result in performing instrumentation of said code block to detect whether execution of said code block results in the misaligned data access.

23. The machine-readable medium of claim 22, wherein the instructions that result in detecting result in performing instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access.

24. The machine-readable medium of claim 21, wherein the instructions that result in detecting result in performing instrumentation of at least one instruction in said code block to detect a location of an instruction whose execution results in the misaligned data access.

25. The machine-readable medium of claim 21, wherein the instructions comprise at least part of a translator.

26. The machine-readable medium of claim 21, wherein the instructions comprise at least part of an execution layer.

27. The machine-readable medium of claim 21, wherein the instructions comprise at least part of an operating system.

28. The machine-readable medium of claim 21, wherein the instructions comprise at least part of a compiler.